Amendments to the Drawings:

The attached replacement sheet of drawings include changes to FIG. 5, and replace the original sheet including FIG. 5.

In FIG. 5, the figure number, title, and block identifiers have been amended to be of uniform character size.

Replacement Sheet (1 page)

REMARKS

Claims 1-19 were pending. Claims 1 and 3 have been amended. Claim 2 has been substantially incorporated into claim 1. Claim 2 has, therefore, been cancelled. Claim 20 is newly submitted. The specification has been amended to correct a typographical error. The Figures have been amended to correspond to the specification. No new matter has been added. Accordingly, claims 1 and 3-20 remain pending. Reconsideration is respectfully requested in view of the amendments to the claims and the following remarks.

I. Drawings

FIG. 5 has been amended such that the figure number, title, and block identifiers are of uniform character size. Applicant respectfully requests withdrawal of the objections to the drawings.

II. Specification

The specification was objected to based on an informality. Applicant has amended the specification as suggested by the Examiner.

III. Allowable Subject Matter

Applicant wishes to thank the Examiner for allowing claims 16-19, and for indicating that claims 14 and 15 recite allowable subject matter.

IV. The § 103 Rejections

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application No. 2001/0010090 ("Boyle") in view of U.S. Patent No. 6,622,291 ("Ginetti") and U.S. Patent Application No. 2004/0006584 ("Vanderweerd").

Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Boyle in view of Ginetti and Vanderweerd, and in further view of U.S. Patent Application No. 2003/0084416 ("Dai").

Claims 3-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boyle in view of Ginetti and Vanderweerd, and in further view of Dai and "Using partitioning to help convergence in the standard-cell design automation methodology", ACM, June 1999 ("Kapadia").

Claims 10-13 stand rejected as being unpatentable over Boyle in view of Ginetti, Vanderweerd, Dai and Kapadia, and in further view of U.S. Patent No. 6,263,478 ("Hahn") and U.S. Patent Application No. 2001/0015658 ("Kousal").

Claim 1, as amended, recites a method for predicting delay of a multi-million gate sub-micron ASIC design. The method includes automatically partitioning a netlist into at least two timing-independent logic cones such that a timing effect of a first logic cone does not propagate to, or affect, a second logic cone in the design. The method also includes running respective instances of a delay prediction application on the timing-independent logic cones on at least two computers in parallel.

A potential advantage of such a method is that by partitioning a netlist into timing-independent logic cones, delay prediction for each logic cone can be run in parallel on multiple (inexpensive) workstations to significantly reduce an amount of time required for delay prediction in a given design (specification p. 5, lines 13-21).

The cited references fail to teach several aspects of claim 1.

A. *Neither Boyle, Ginetti, Vanderweerd nor Dai Discloses "Partitioning A Netlist Into At Least Two Timing-Independent Logic Cones" as recited in Claim 1*

The Examiner recognizes that neither Boyle, Ginetti, nor Vanderweerd discloses partitioning a netlist into timing-independent logic cones, however, the Examiner asserts that this limitation is disclosed by Dai. In particular, in rejecting claim 2, the Examiner cites the Abstract, and paragraphs 0034, 0036 and 0039 of Dai as disclosing partitioning a net list into timing-independent partitions. Applicant respectfully disagrees.

In the cited portion, Dai discloses dividing a netlist into separate partitions, and then independently laying out each partition so that each partition satisfies a given spatial and timing constraint (pg. 4, para 0039). In particular, Dai discloses a partitioning engine that divides a design such that a signal path between two nodes can extend across partition boundaries (pg. 8, para 90). Because a signal path can extend across partition boundaries, a timing effect of one partition will, therefore, propagate, or affect, the other partition. In contrast, claim 1 requires, automatically partitioning a netlist into at least two timing-independent logic cones such that a timing effect of a first logic cone does not propagate to, or affect, a second logic cone in the design (emphasis added).

Moreover, because each of Dai's partitions are independently laid out to satisfy a given spatial and timing constraint, it is not inherent that each of Dai's partitions are timing-independent as recited in claim 1. *See* MPEP 2163.07 - "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

B. *Boyle Fails to Disclose "Running Respective Instances of a Delay Prediction Application" as recited in Claim 1*

In rejecting claim 1, the Examiner cites page 2, paragraph 0014, page 3, paragraph 38, page 4, paragraph 48 and page 5, paragraph 0049 as disclosing running respective instances of a delay prediction application on at least two computers in parallel. Applicant respectfully disagrees.

Boyle, instead, discloses performing in parallel placement, logic optimization and routing functions using only a *single* computer system that contains multiple CPUs (pg. 4, para 48; FIG. 4). In contrast, claim 1, requires running respective instances of a delay prediction application on the timing-independent logic cones on at least two computers in parallel. As indicated above, a potential advantage of the Applicant's method is that delay prediction (in a multi-million gate sub-micron ASIC design) can be performed using inexpensive workstations. Claim 1 is, therefore, allowable over Boyle, Ginetti, Vanderweerd and Dai (either alone or in combination).

Claims 3-7 depend from claim 1, and are allowable over Boyle, Ginetti, Vanderweerd and Dai for at least the reasons set forth with those of claim 1.

Claim 8 (and the claims that depend therefrom) incorporate limitations similar to claim 1, and are also allowable over Boyle, Ginetti, Vanderweerd and Dai for at least the reasons set forth with those of claim 1.

In view of the foregoing, it is submitted that the claims 1 and 3-20 are allowable over the references cited above, and are in condition for allowance. Should any unresolved issues remain, the Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,
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